67,200-327
Serial Number 09/885,784

In the Claims

Please cancel claims 1 and 14-15.

Please amend claims 2-6, 8 and 11-13 as follows.

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2. (Amended) The method of claim 11 wherein the microelectronic device is selected from the group consisting of resistors, transistors, diodes and capacitors.

3. (Amended) The method of claim 11 wherein the second substrate is selected from the group consisting of conductor substrates, semiconductor substrates, dielectric substrates and aggregates thereof.

4. (Amended) The method of claim 11 wherein the second substrate is a second semiconductor substrate.

5. (Amended) The method of claim 11 wherein the first semiconductor substrate is thicker than the second substrate.

6. (Amended) The method of claim 11 wherein the dielectric isolated metallization pattern comprises a plurality of laminated patterned conductor layers.

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8. (Amended) The method of claim 11 wherein the mating of the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern formed over the second substrate is undertaken while employing a

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laminating method selected from the group consisting of thermally assisted laminating methods and pressure assisted laminating methods.

11. (Amended) A method for fabricating a semiconductor integrated circuit microelectronic fabrication comprising:

providing a first semiconductor substrate;

forming over the first semiconductor substrate at least one microelectronic device to form from the first semiconductor substrate a partially fabricated semiconductor integrated circuit microelectronic fabrication;

providing a second substrate;

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forming over the second substrate, in inverted order, a dielectric isolated metallization pattern intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication;

laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the second substrate to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern to thus form a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication; and

removing the second substrate from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods, said planarizing methods employ said dielectric isolated metallization pattern as a stop layer.